

APPENDIX

IN THE CLAIMS

1. A liquid crystal display comprising:

a display portion in which a plurality of pixels are two-dimensionally arranged at intersecting points of gate lines as many as a plurality of rows and signal lines as many as a plurality of columns which are wired in a matrix shape; and

a plurality of driver circuits for applying a signal potential to each pixel in said display portion through the signal lines of said plurality of columns,

characterized in that when said plurality of driver circuits are arranged in order while the numbers of output terminals of said driver circuits are set to a same number so as to have a correspondence relation with each of the signal lines of said plurality of columns, if a fraction occurs in the signal lines of said plurality of columns, the number of output terminals of one of said plurality of driver circuits is set to said fraction.

2. A display according to claim 1, characterized in that said plurality of driver circuits are driver ICs arranged in

an outside of a transparent insulating substrate on which said display portion is formed.

3. A liquid crystal display comprising:

a display portion in which a plurality of pixels are two-dimensionally arranged at intersecting points of gate lines as many as a plurality of rows and signal lines as many as a plurality of columns which are wired in a matrix shape; and

a plurality of driver circuits for applying a signal potential to each pixel in said display portion through the signal lines of said plurality of columns,

characterized in that the number of output terminals of each of said plurality of driver circuits is set to a measure of the total number of signal lines of said plurality of columns.

4. A display according to claim 3, characterized in that the number of output terminals of each of said plurality of driver circuits is set to a same number.

5. A display according to claim 3, characterized in that the number of output terminals of each of said plurality of driver circuits is set to a power of 2.

6. A display according to claim 3, characterized in

that said plurality of driver circuits are driver ICs arranged in an outside of a transparent insulating substrateon which said display portion is formed.

7. A display according to claim 3, characterized by comprising:

a memory circuit for temporarily storing data to be written into said plurality of driver circuits; and

a control circuit for controlling said plurality of driver circuits so as to simultaneously write different data from said memory circuit.

8. A display according to claim 4, characterized in that when a size of a frame portion adjacent to said display portion is specified, the number (n) of output terminals of each of said plurality of driver circuits is determined on the basis of said specified frame size by the number of lines which can be wired into a wiring region of said frame portion.

9. (amended) A display according to claim 8, characterized in that when ~~it is assumed that~~ the total number of signal lines of said plurality of columns which is decided by a display system is set to N, the number of said driver circuits is set to  $N/n$ .

10. A display according to claim 3, characterized by comprising:

time-divisional switches for time-divisionally sending a signal potential which is outputted from each of said plurality of driver circuits to the signal lines of said plurality of columns.

11. A display according to claim 10, characterized in that a leading waveform and a trailing waveform of a signal output waveform of each of said plurality of driver circuits are symmetrical with respect to a time base.

12. A display according to claim 10, characterized in that a time-dividing number of said time-divisional switches is equal to 3.

13. A display according to claim 12, characterized in that a period of time which is selected by said time-divisional switches is equal to or shorter than 1/3 of a horizontal scanning period.

14. A display according to claim 13, characterized in that a leading time and a trailing time of each of said plurality

of driver circuits are equal to or shorter than the period of time which is selected by said time-divisional switches.

15. A display according to claim 13, characterized in that a blanking period which is caused for the period of time, selected by said time-divisional switches is equal to or shorter than (a horizontal scanning period - the period of time selected by the time-divisional switches  $\times$  3) / 3.

16. (amended) A display according to claim 15, characterized in that said plurality of driver circuits have a function to stop the operation of an their output circuit of said plurality of driver circuits for said blanking period.

17. A display according to claim 12, characterized in that said plurality of driver circuits generate a signal potential so as to correct curves of voltage-transmittance characteristics of R (red), G (green), and B (blue) by diving to said time-divisional switches.

18. A display according to claim 12, characterized in that in a 1H (H denotes a horizontal scanning period) inversion driving or a 1H common inversion driving, the signal line which is selected first by said time-divisional switches is a line of

blue, the signal line which is selected at the second time is a line of green, and the signal line which is selected at the third time is a line of red.

19. A display according to claim 10, characterized in that in a dot inversion driving, the signal line which is selected first by said time-divisional switches is a line of red, the signal line which is selected at the second time is a line of green, and the signal line which is selected at the third time is a line of blue.

20. A display according to claim 12, characterized in that time-division of said time-division switches distribute signals to R (red), G (green), and G (blue) constituting one pixel.

Please add the following new claims.

21. (new) A display according to claim 1, characterized in that a surplus connecting region that does not contribute to said display portion does not occur on the said display.

22. (new) A display according to claim 1, characterized in that a driver circuit of said plurality of driver circuits is

separate and distinct from another driver circuit of said plurality of driver circuits.

23. (new) A display according to claim 3, characterized in that a surplus connecting region that does not contribute to said display portion does not occur on the said display.

24. (new) A display according to claim 3, characterized in that a driver circuit of said plurality of driver circuits is separate and distinct from another driver circuit of said plurality of driver circuits.

25. (new) A liquid crystal display comprising:  
a display portion, said display portion having a plurality of gate lines, a plurality of signal lines and a plurality of pixels, a pixel of said plurality of pixels being located at an intersection of a gate line of said plurality of gate lines and a signal line of said plurality of signal lines; and

a plurality of driver circuits, a driver circuit of said plurality of driver circuits being separate and distinct from another driver circuit of said plurality of driver circuits, each driver circuit of said plurality of driver circuits having a plurality of output terminals, said plurality

of output terminals providing a plurality of signal potentials to a group of signal lines of said plurality of signal lines, said group of signal lines being less than all of said plurality of signal lines.

26. (new) A display according to claim 25, wherein said each driver circuit is separate and distinct from another driver circuit of said plurality of driver circuits.

27. (new) A display according to claim 25, wherein said plurality of pixels are arranged in a two-dimensional matrix shape.

28. (new) A display according to claim 25, wherein said pixel of said plurality of pixels includes a transistor, a gate electrode of said transistor being electrically connected to said gate line, a source/drain of said transistor being electrically connected to said signal line.

29. (new) A display according to claim 25, wherein said plurality of gate lines is a plurality of rows and said plurality of signal lines is a plurality of columns.

30. (new) A display according to claim 25, wherein an

output terminal of said plurality of output terminals provides a signal potential of said plurality of signal potentials to said signal line.

31. (new) A display according to claim 25, wherein a surplus connecting region that does not contribute to said display portion does not occur on the said display.

32. (new) A display according to claim 25, wherein an amount of signal lines of said plurality of signal lines is connected to said driver circuit, said amount being an integer not less than 1.

33. (new) A display according to claim 32, wherein another amount of signal lines of said plurality of signal lines is connected to said another driver circuit, said amount being equal to said another amount, said another amount being an integer not less than 1.

34. (new) A display according to claim 32, wherein a remainder amount of said plurality of signal lines is less than said amount of said plurality of signal lines, said remainder amount being the amount of said plurality of signal lines connected to a remainder driver circuit of said plurality of

driver circuits, each other driver circuit of said plurality of driver circuits being connected to said amount of said plurality of signal lines.

35. (new) A display according to claim 34, wherein another amount of said output terminals is the amount of said output terminals for said another driver circuit, and said amount is equal to said another amount.

36. (new) A display according to claim 35, wherein the aggregate number of output terminals of said plurality of driver circuits is set to a measure of the total number of said signal lines.

37. (new) A display according to claim 36, wherein an output terminal of said plurality of output terminals is electrically connected to an input terminal of a time-divisional switch, said time-divisional switch providing a signal potential of said plurality of signal potentials to said signal line as a de-multiplexed signal potential.

38. (new) A display according to claim 35, wherein said time-division switch distributes said plurality of signal potentials as a red signal potential, a green signal potential

and a blue signal potential.

39. (new) A display according to claim 38, wherein said red signal potential is applied to a red pixel of said plurality of pixels, said green signal potential is applied to a green pixel of said plurality of pixels and said blue signal potential is applied to a blue pixel of said plurality of pixels.